

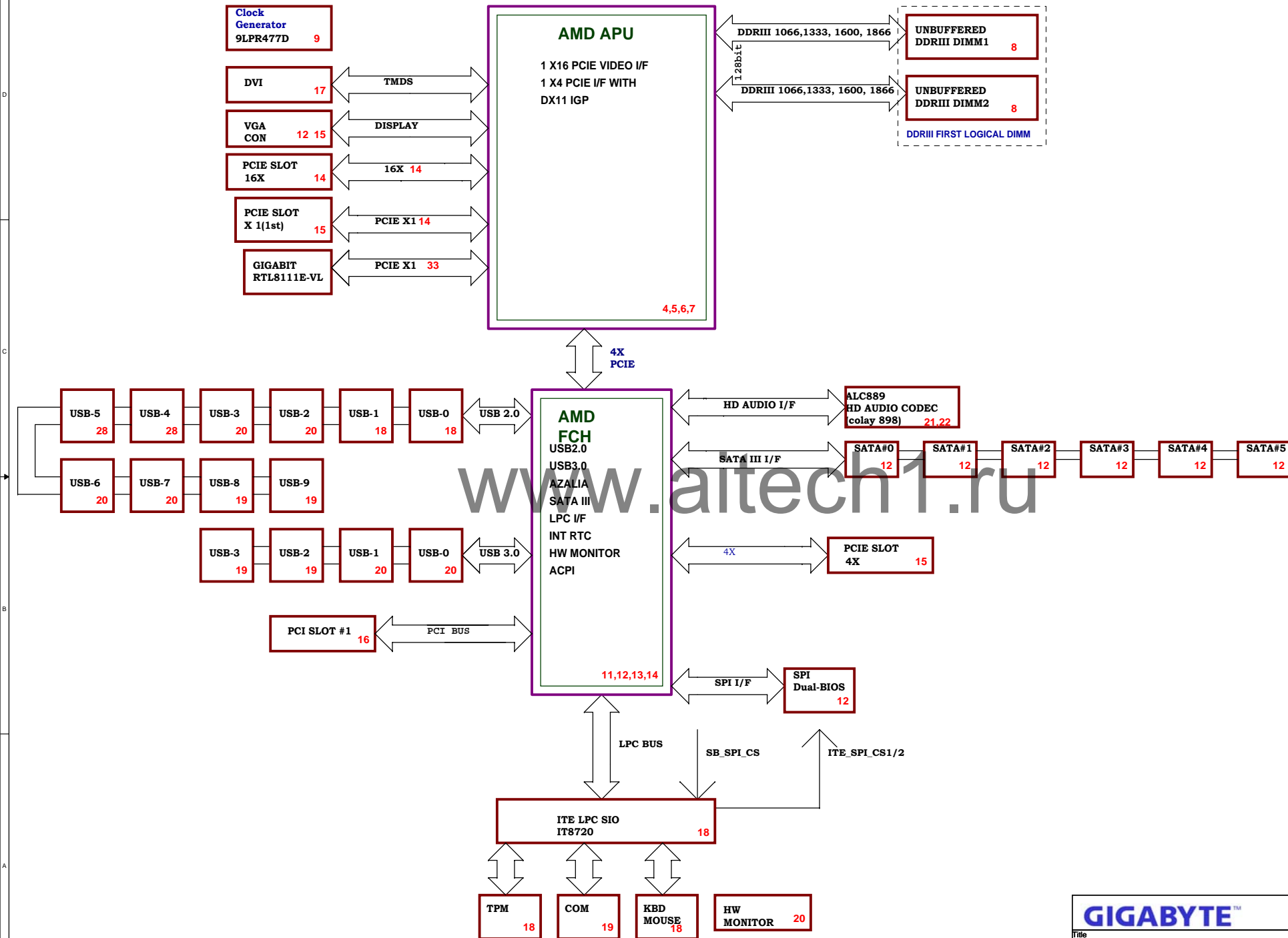
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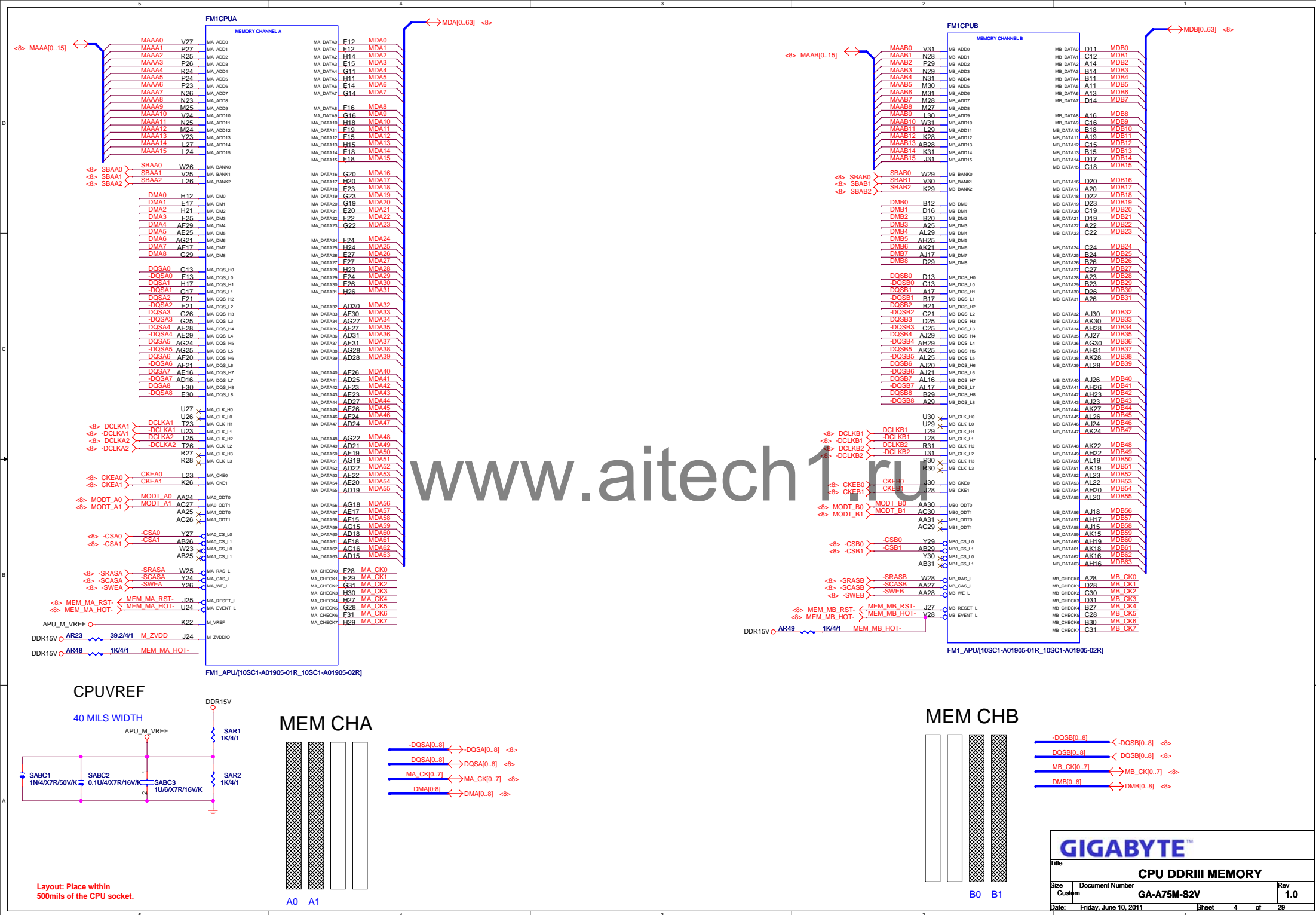
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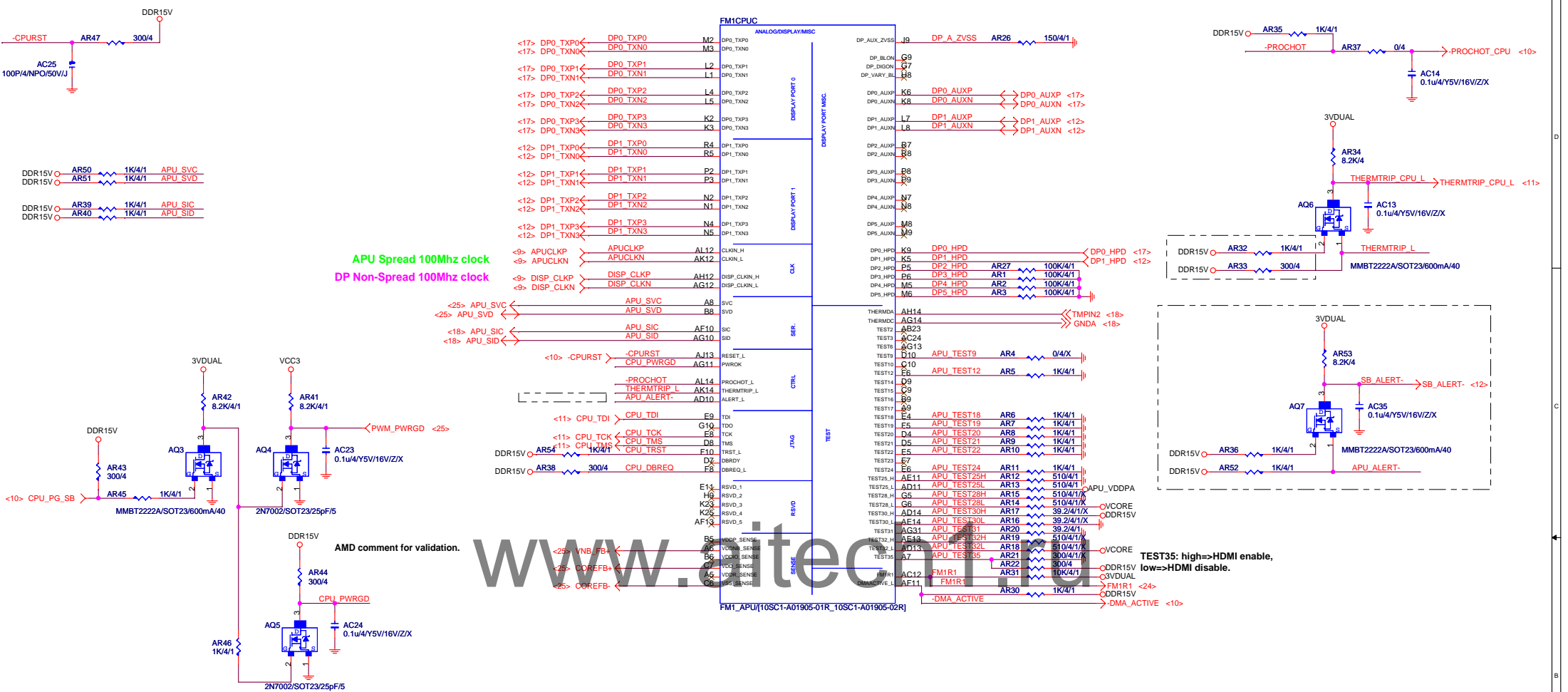
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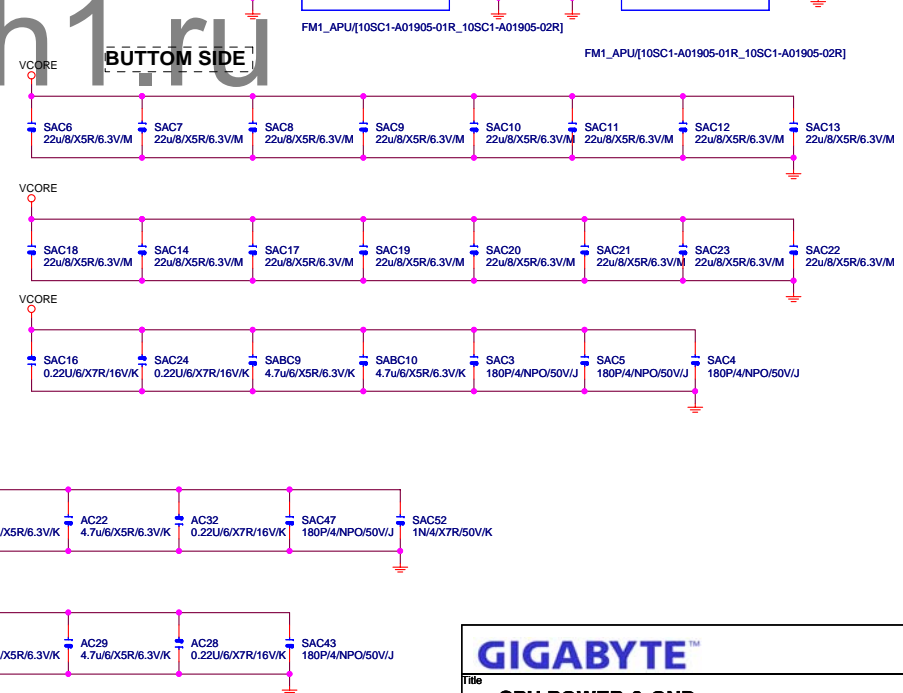
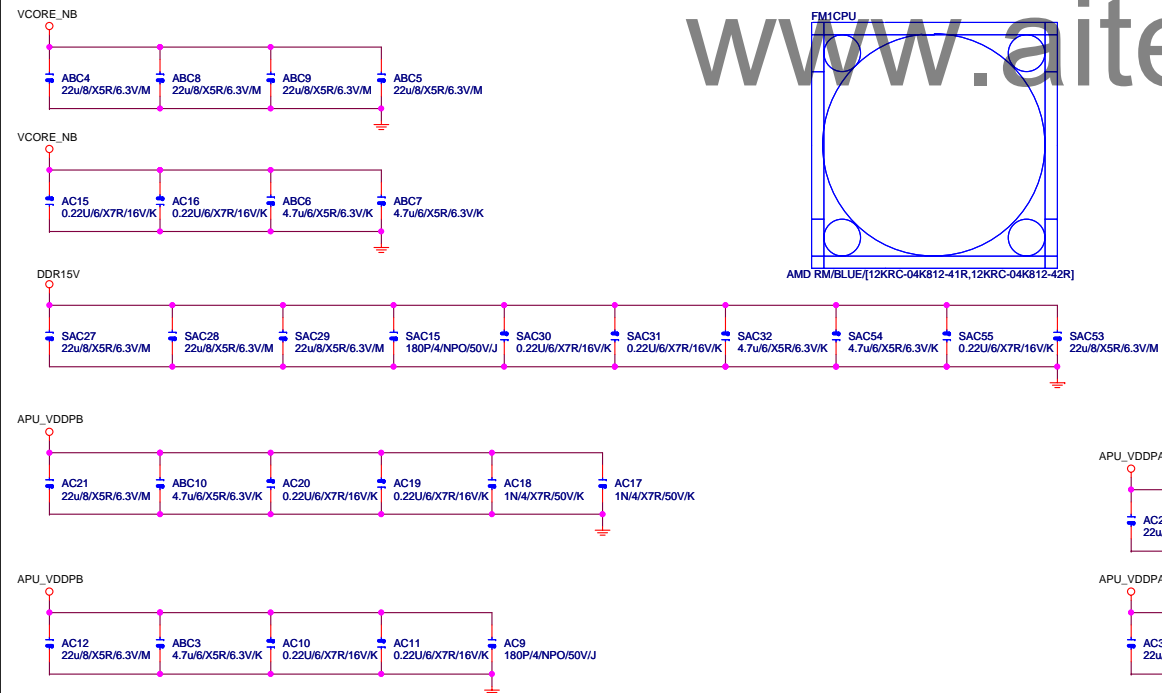
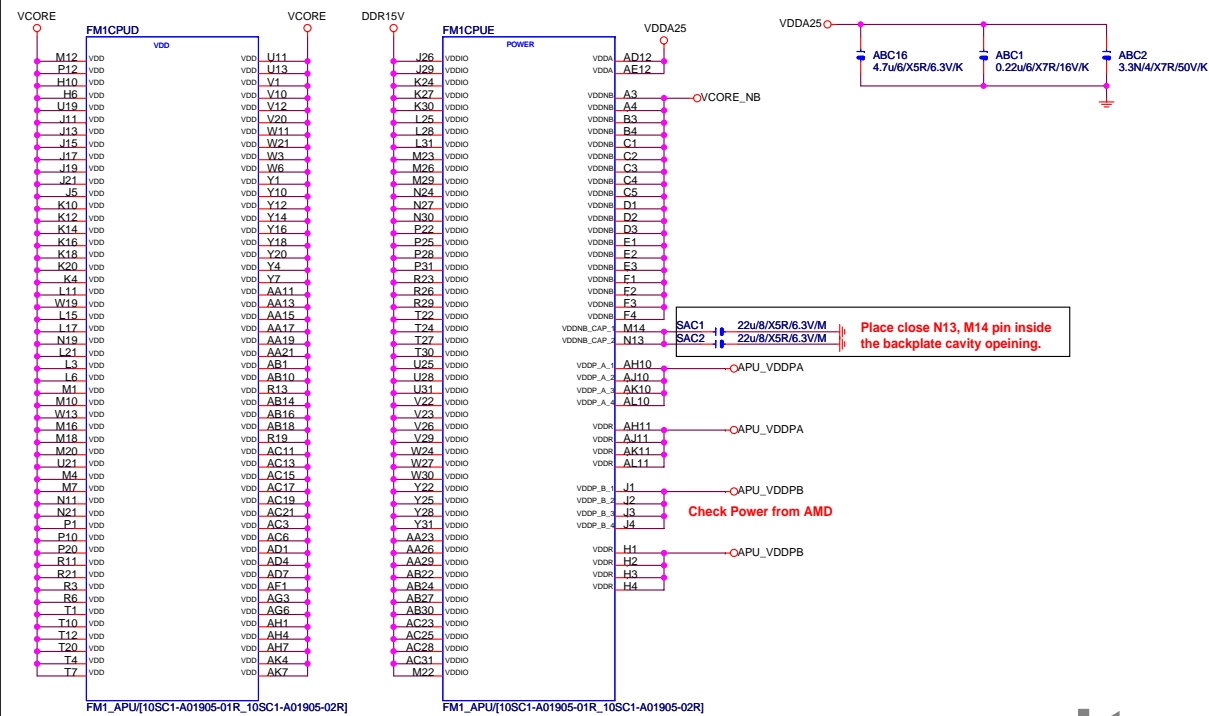
AMD Fusion D3 DESKTOP REFERENCE DESIGN

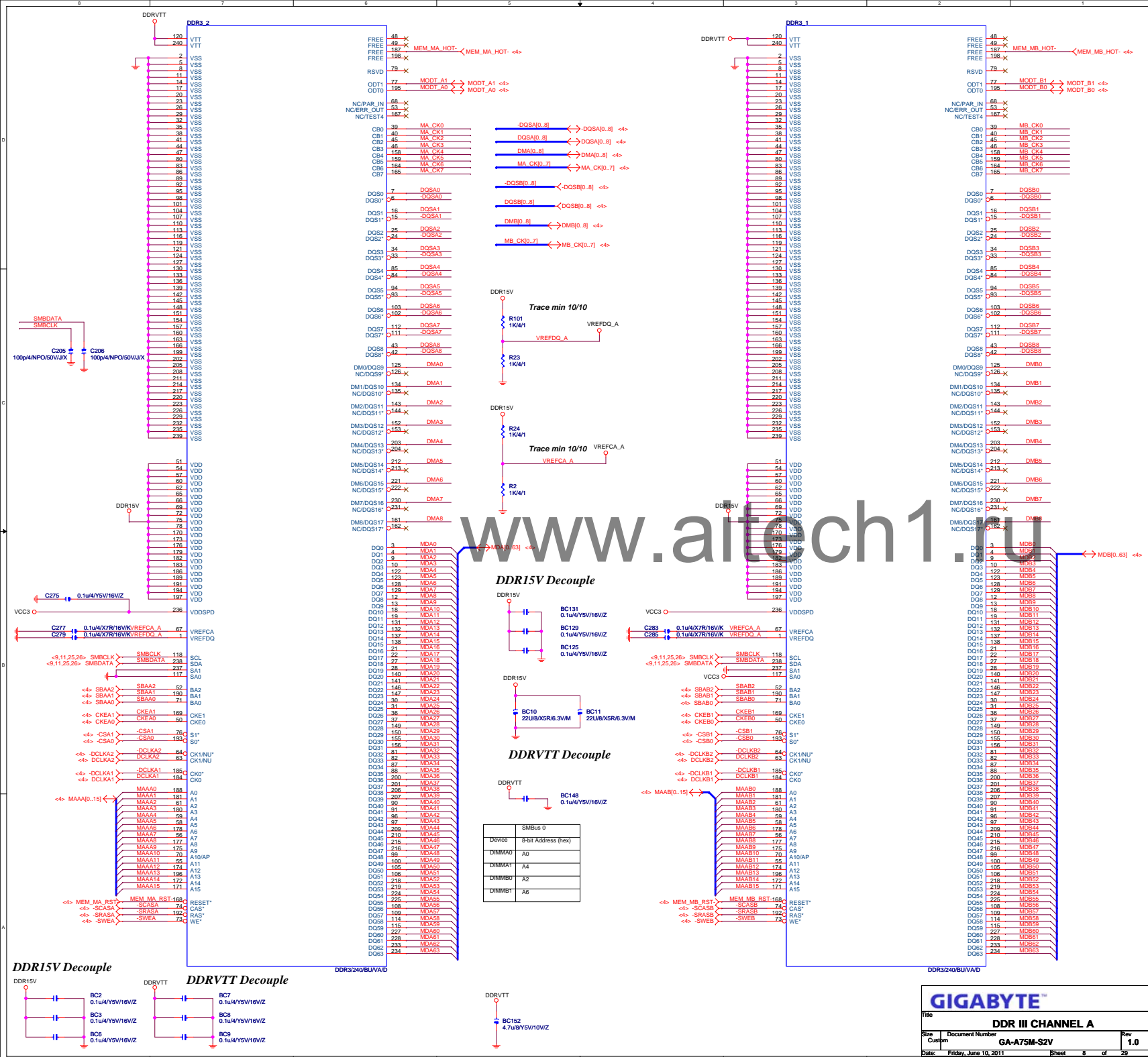


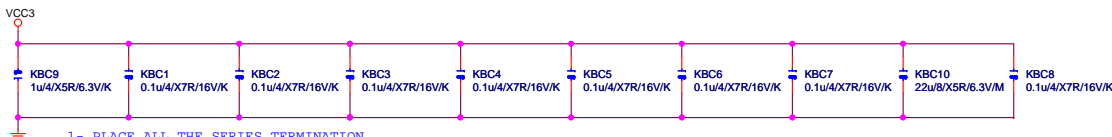




DDR15V=1.25V/1.35V(DDR3)







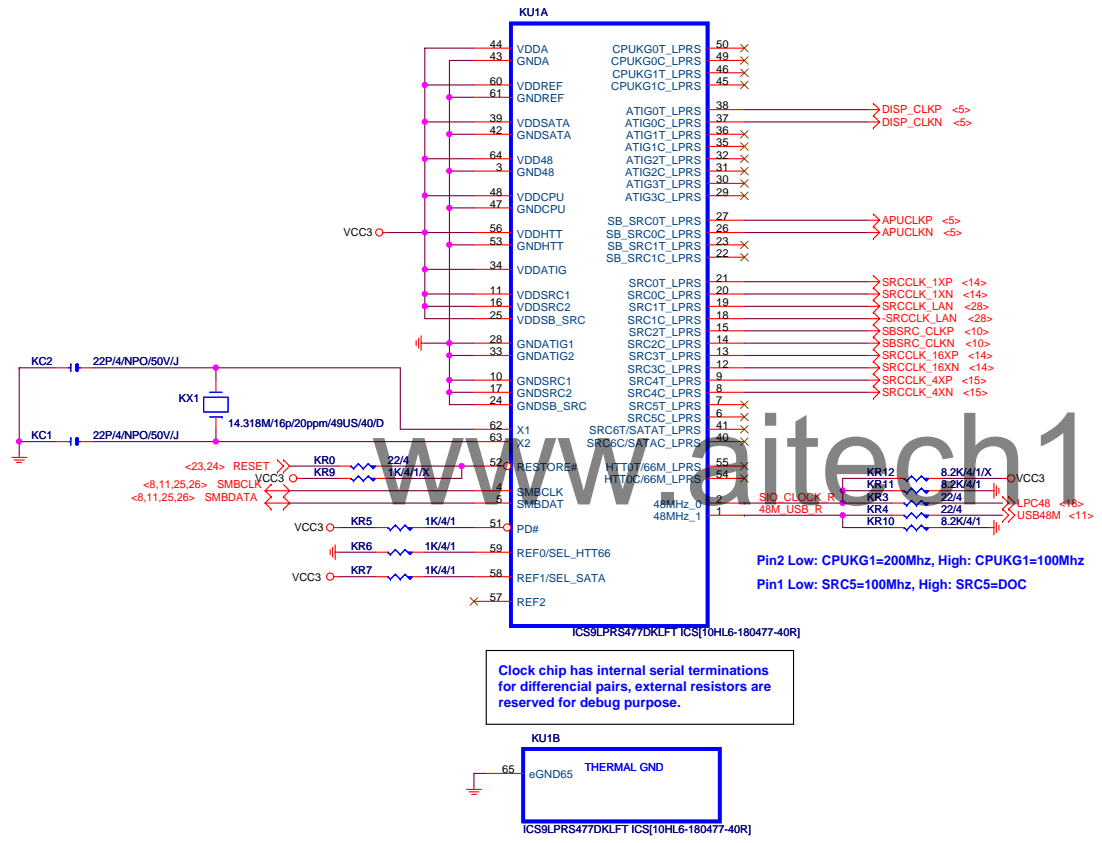
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

watch dog --
RESTORE# 按 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

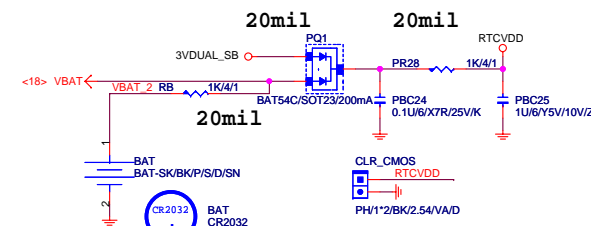
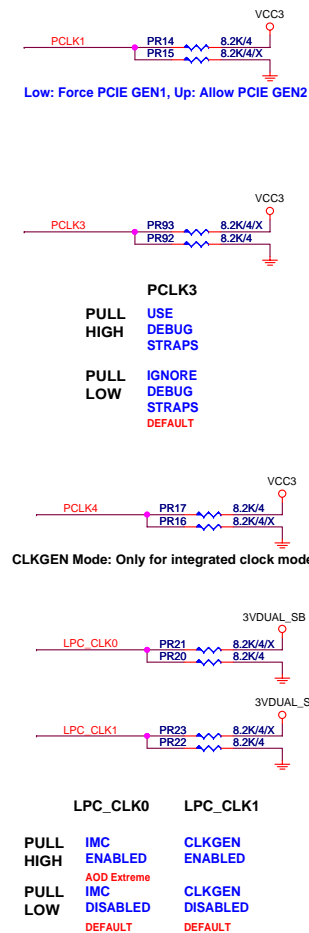
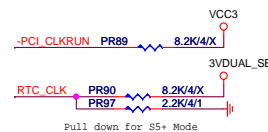
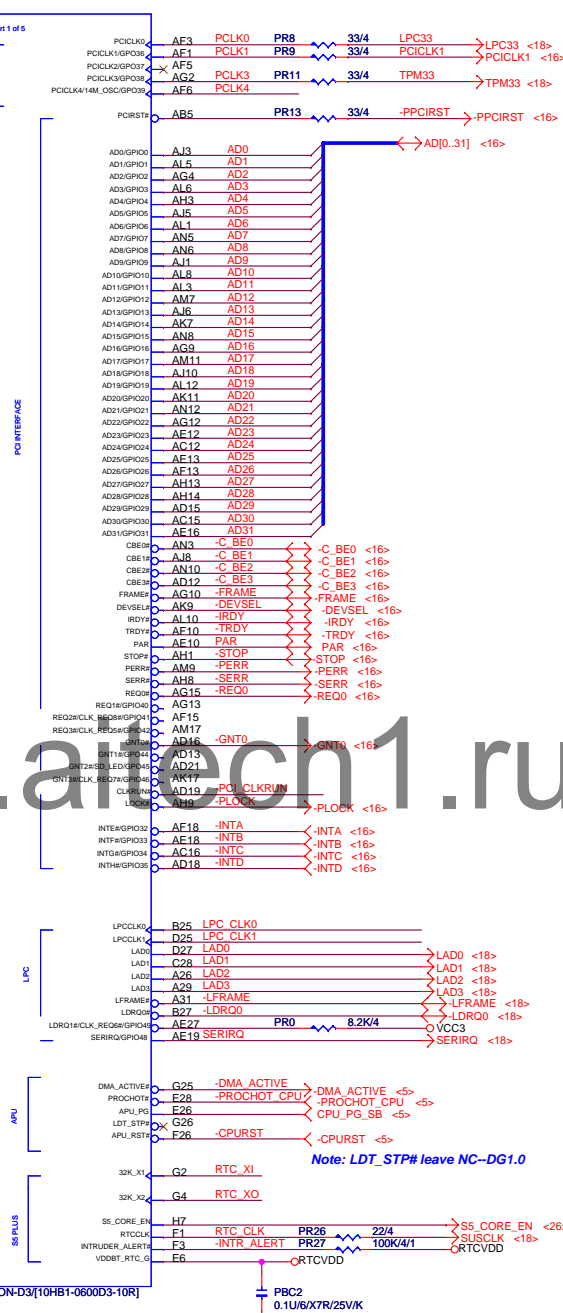
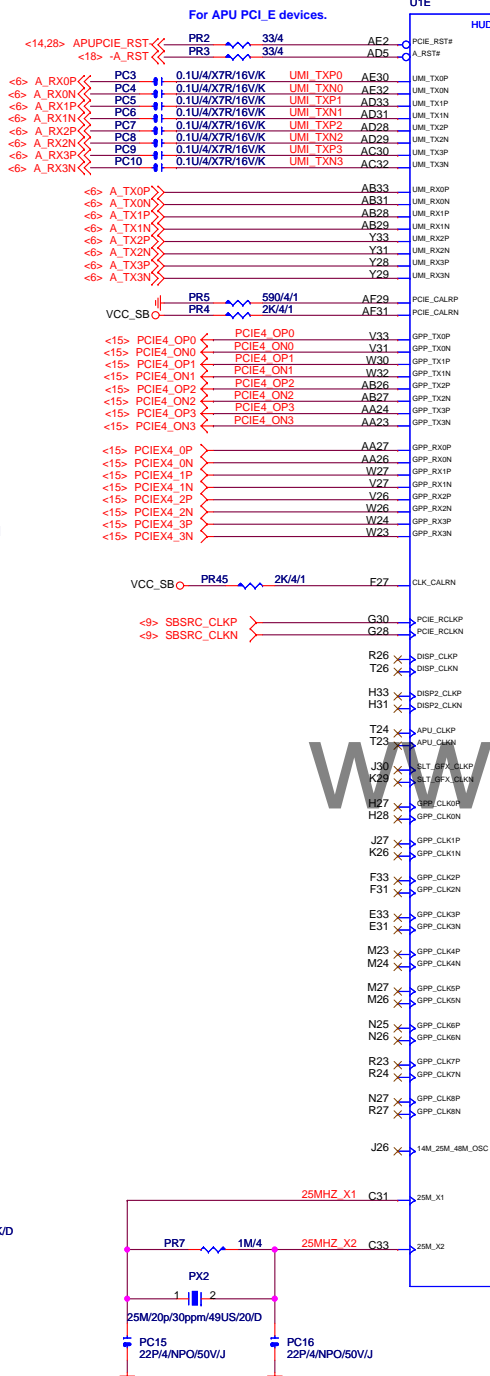
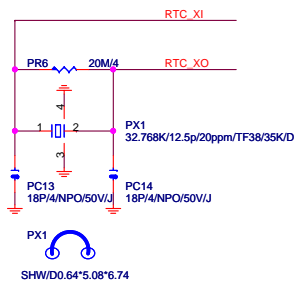
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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Title			ICS9LPRS477CLKF		
Size	Document Number		Rev		
Custom	GA-A75M-S2V		1.0		
Date:	Friday, June 10, 2011	Sheet	9	of	29



Diagram illustrating a square loop structure. The top node is labeled SB_HS. The bottom node is labeled SA0501-01R_12SP2-SA0501-02R_12SP2-SA0501-03R. The loop is formed by four nodes connected by lines, with a vertical line segment on the right side.

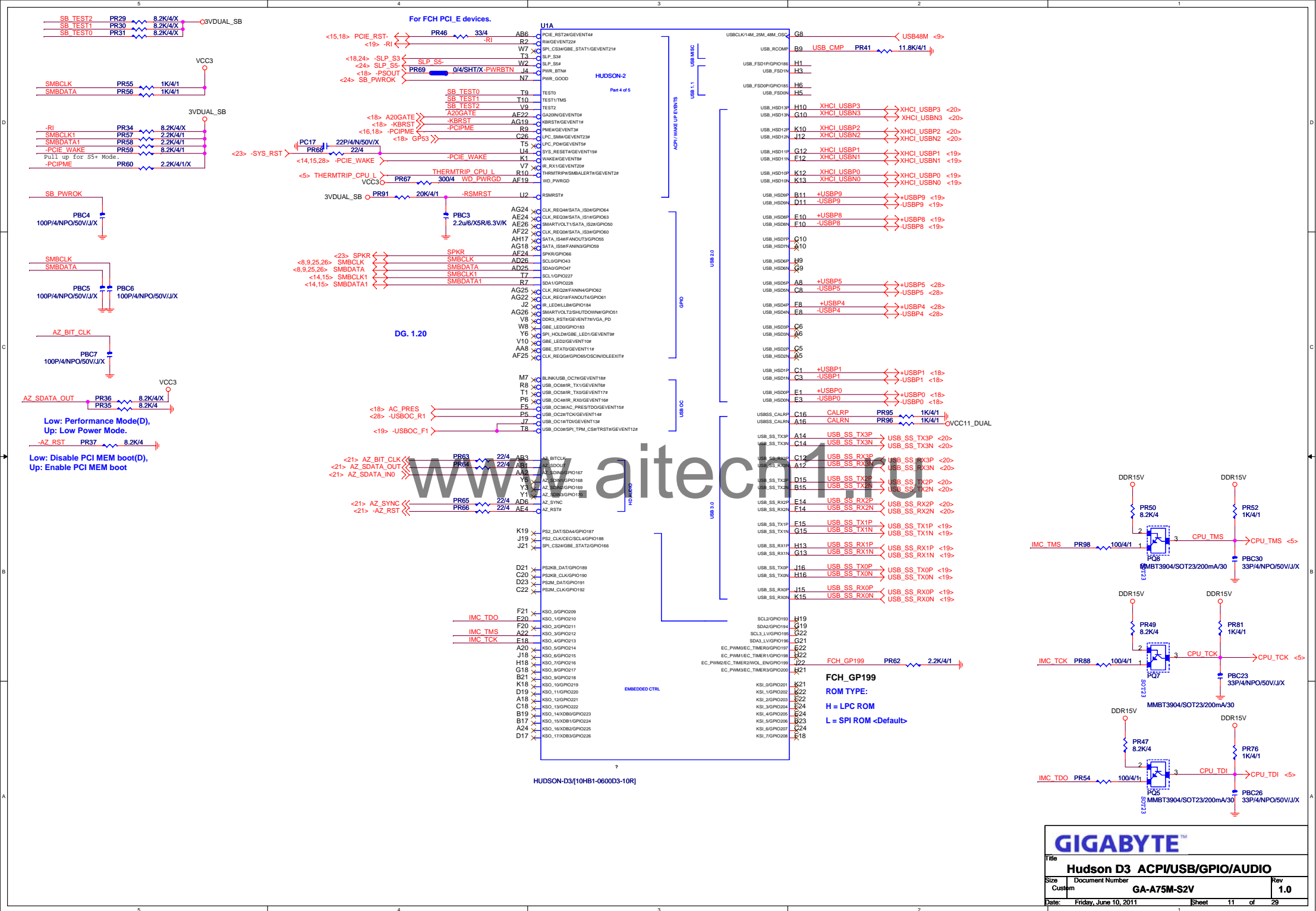


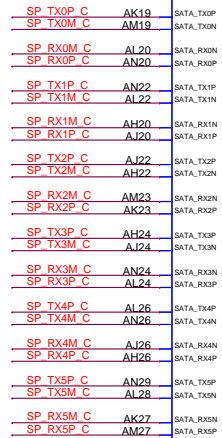
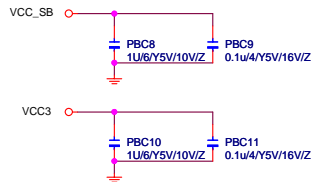
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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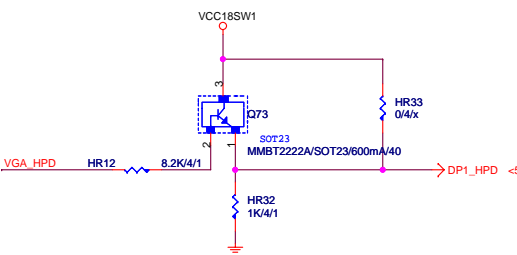
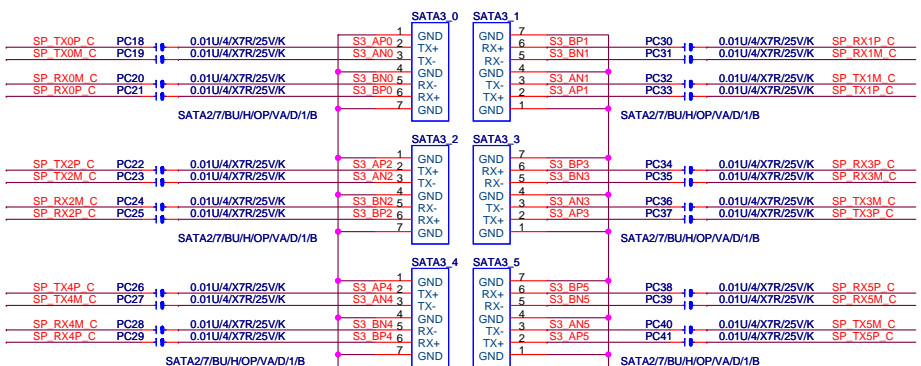
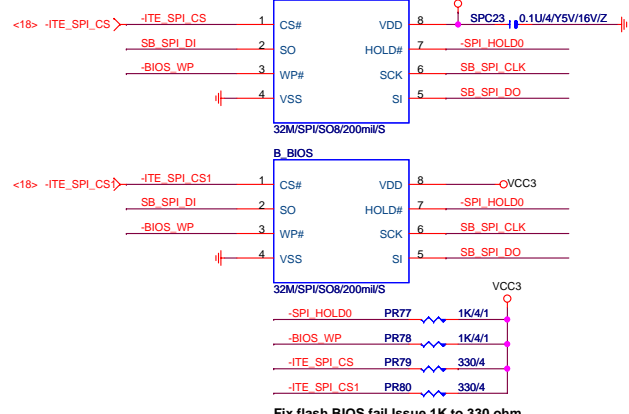
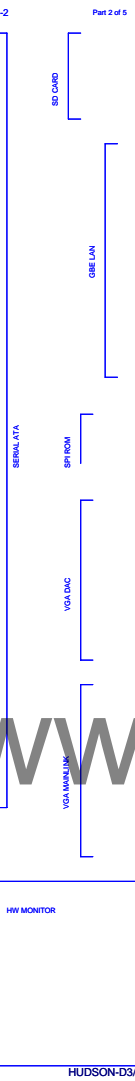
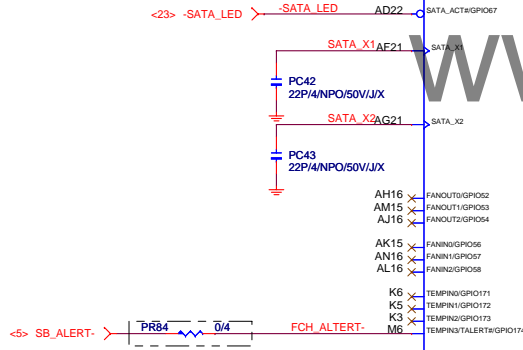
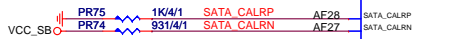
Title			
Hudson D3 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-A75M-S2V	1.0	
Date:	Friday, June 10, 2011	Sheet	10 of 29



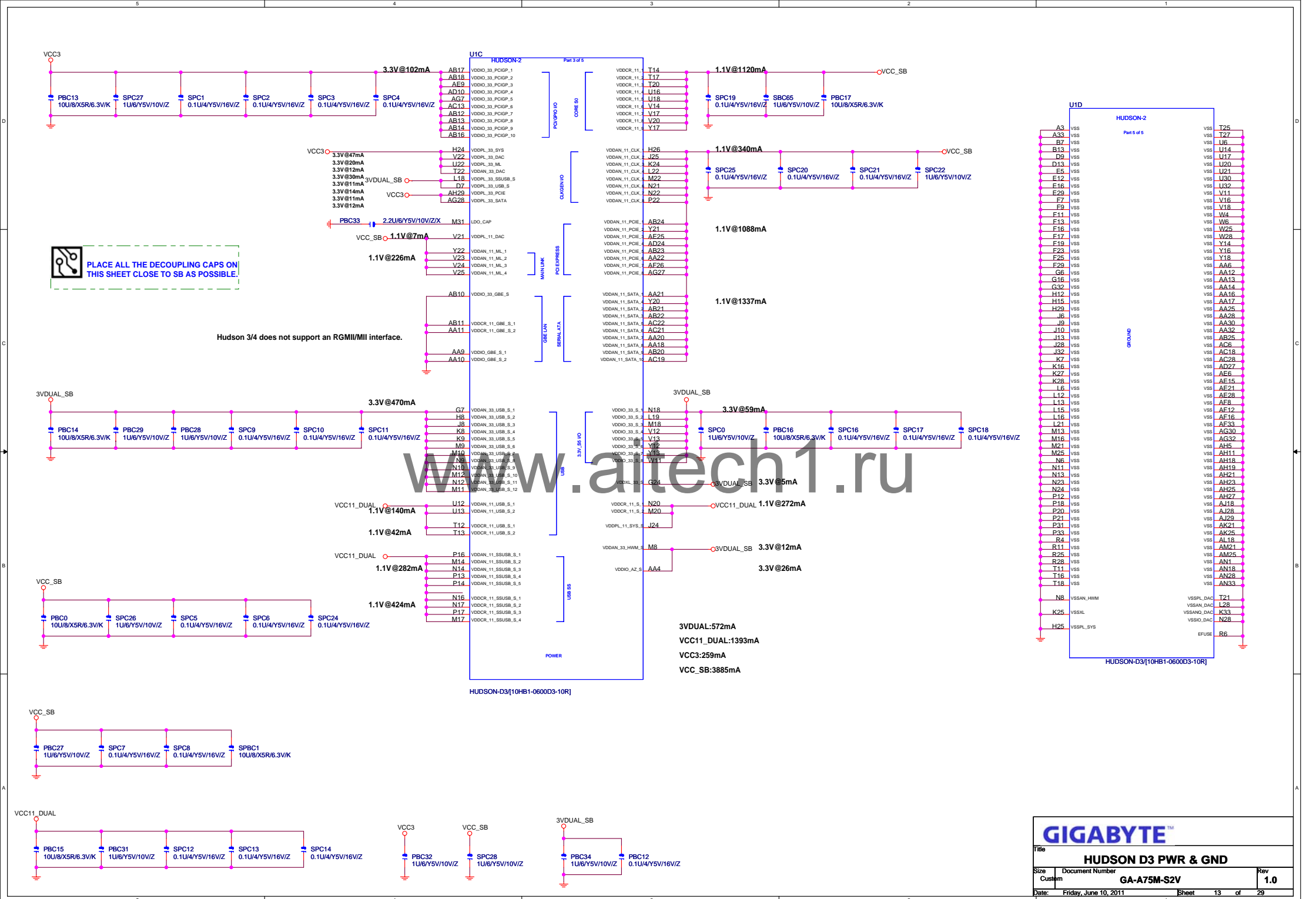


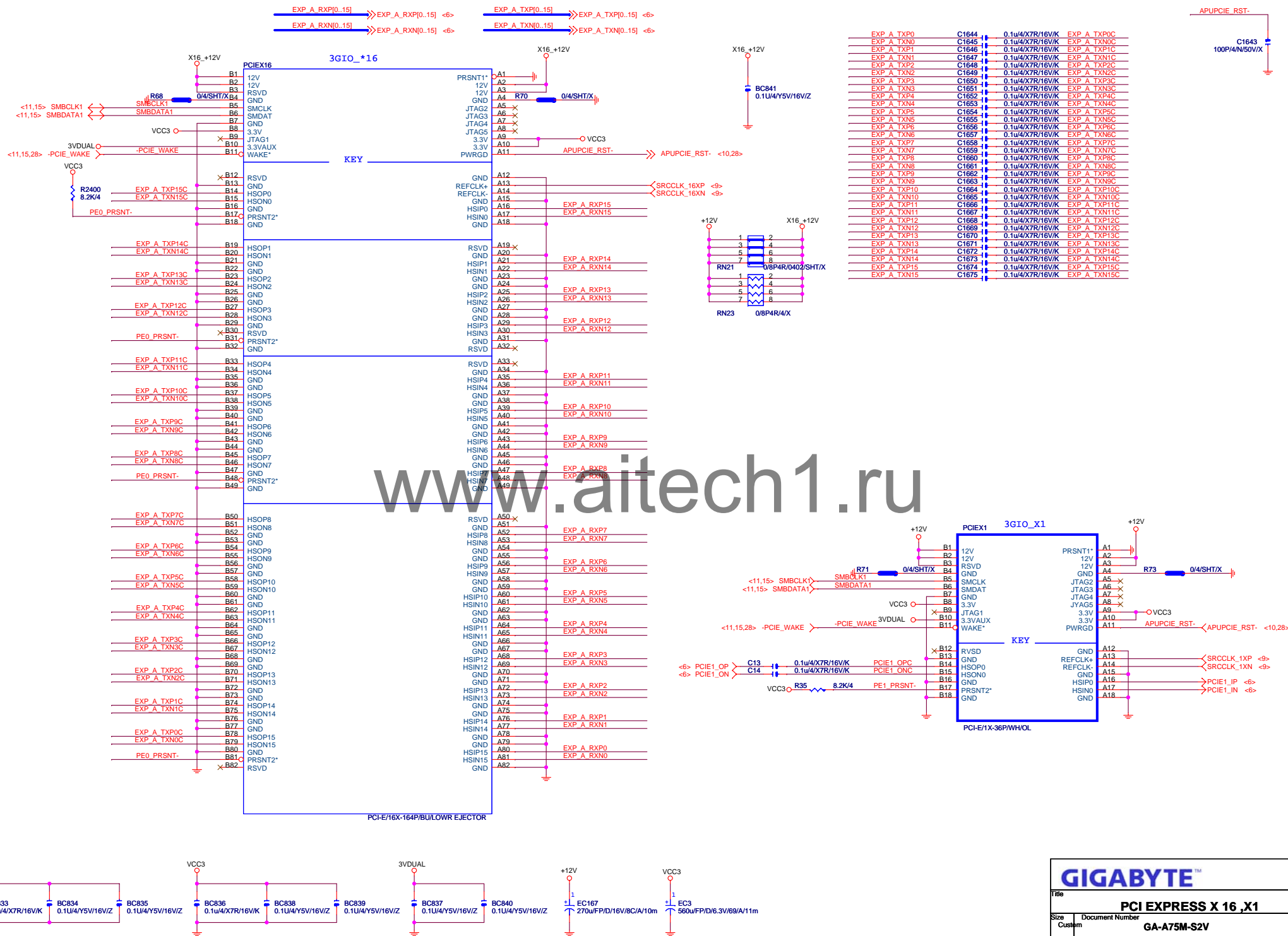
SATA 6-7 for Hudson D4.

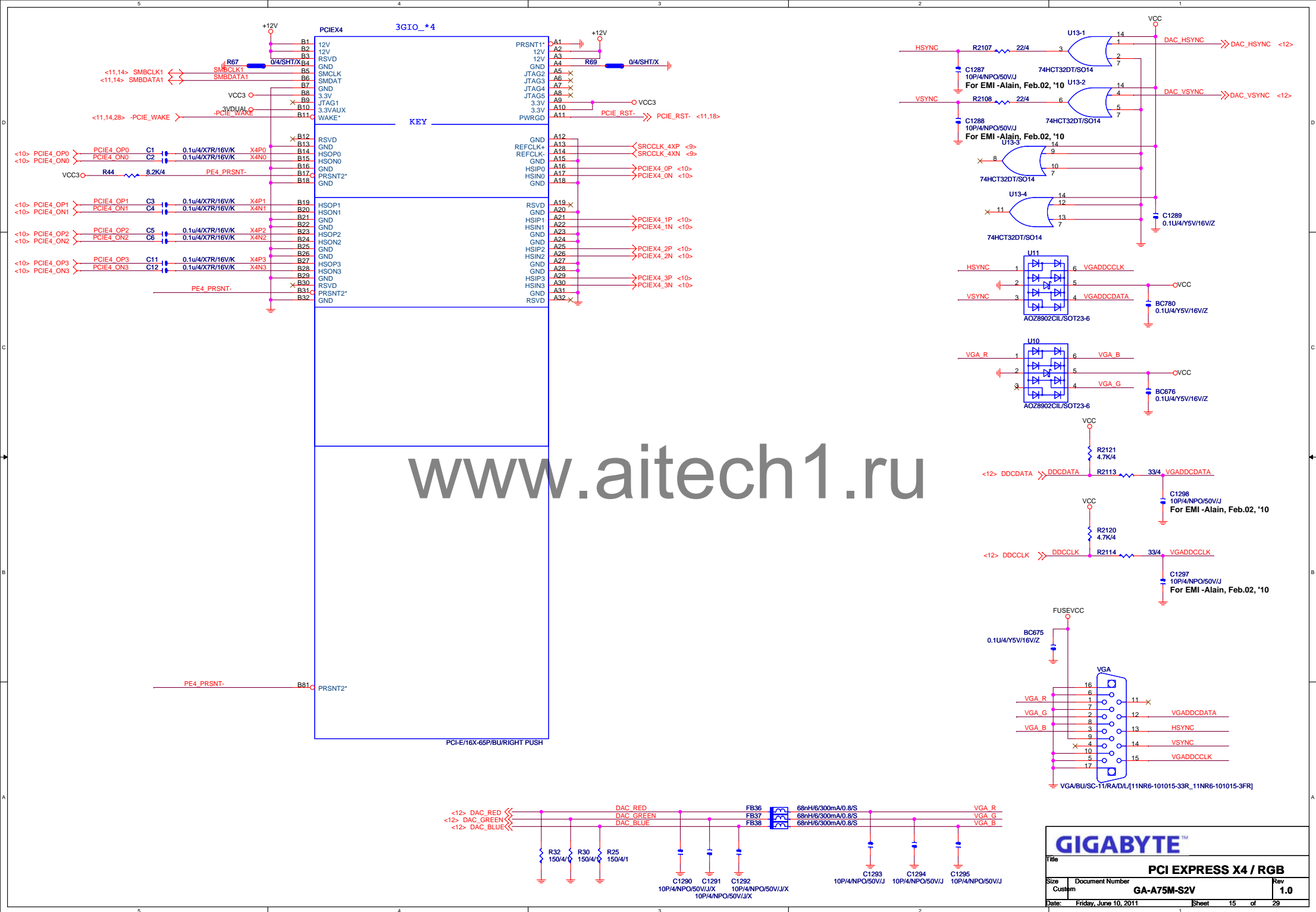
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1

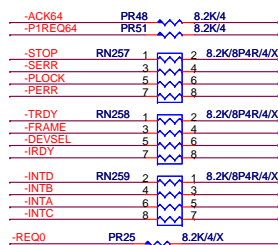


GIGABYTE™			
Title Hudson D3 SATA/HWM/SPI			
Size	Document Number	Rev	
Custom	GA-A75M-S2V	1.0	
Date:	Friday, June 10, 2011	Sheet	12 of 29

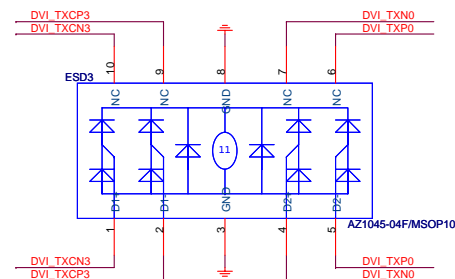
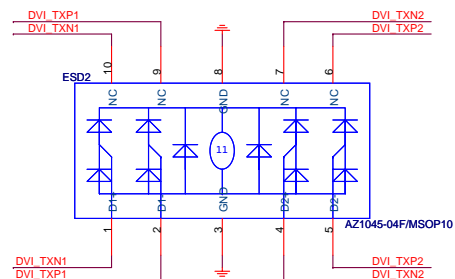
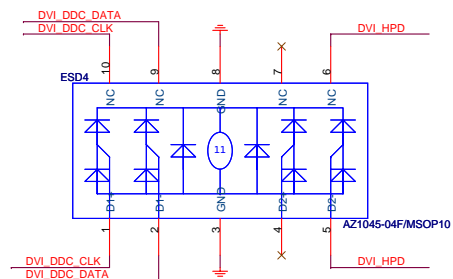
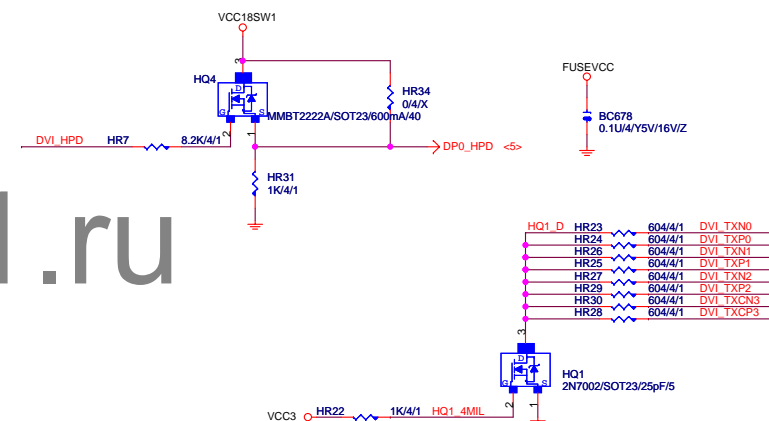
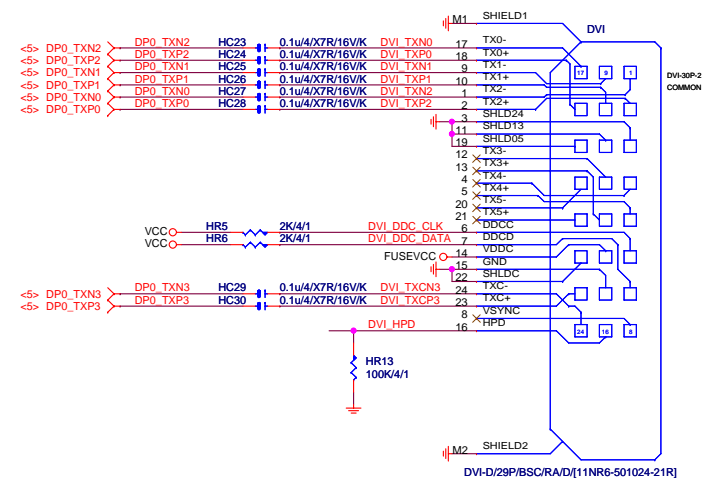
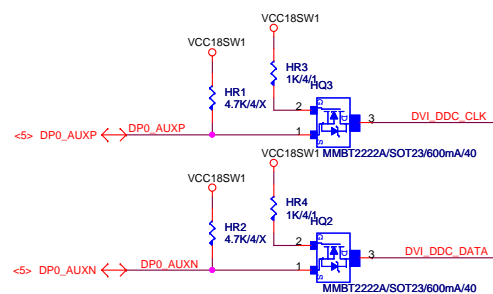


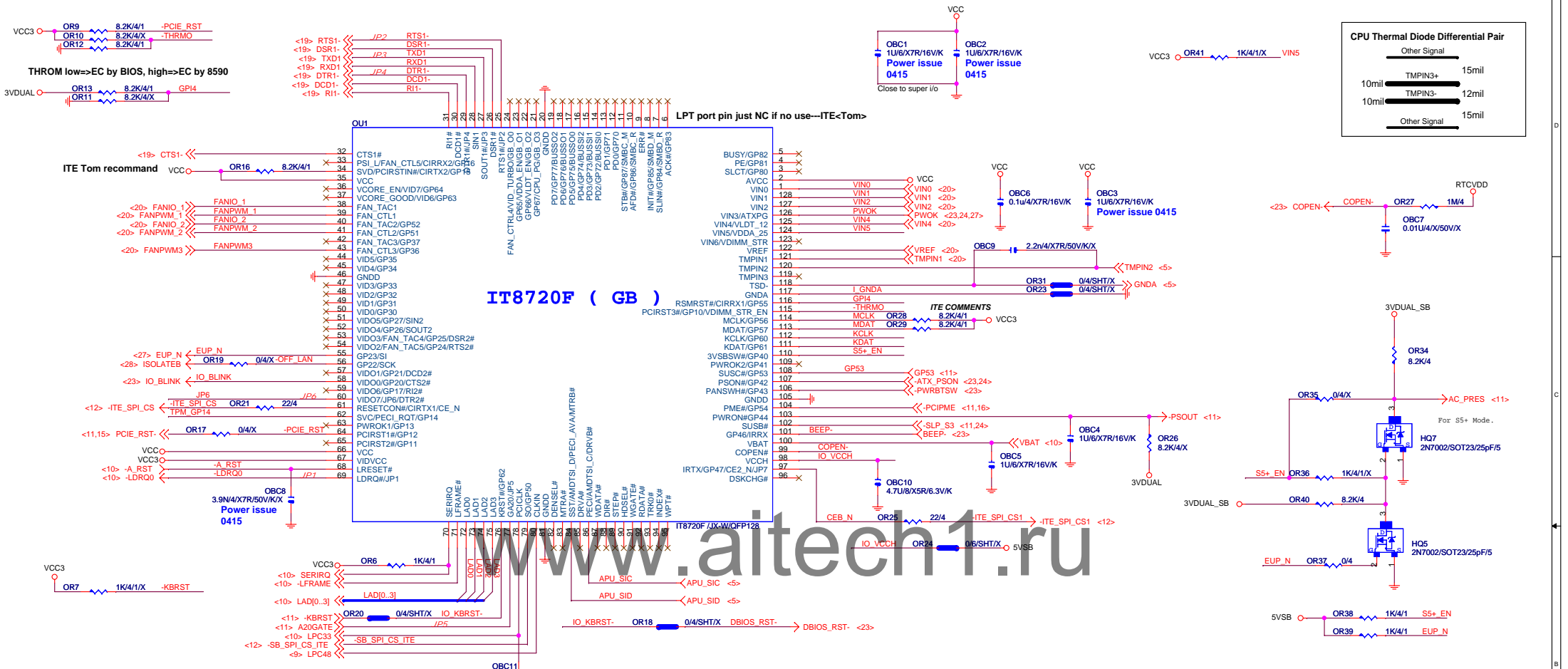




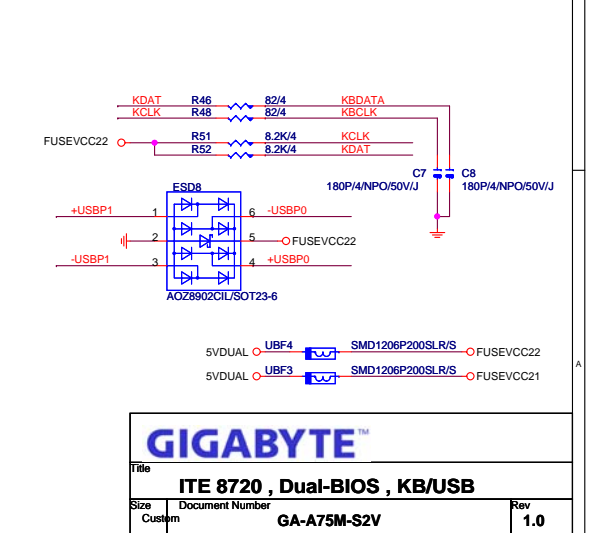
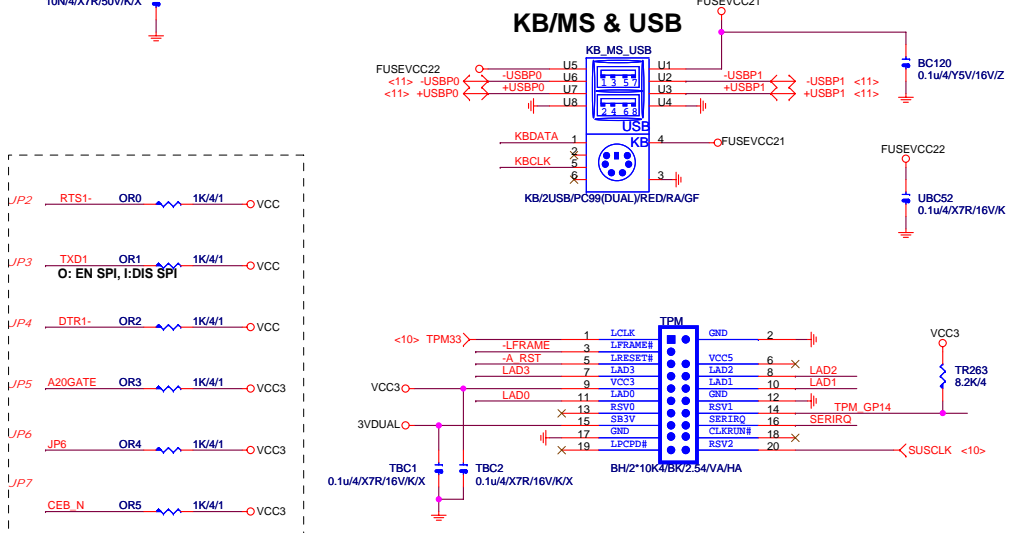


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Symbol	value	Description
JP1 Pin 69		
JP2 Pin 25	VIDO_EN	1 Disable VID output pins 0 Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1 Disabled. 0 Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1 K8 power sequence disabled 0 K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run Default value of EC Index 15h/16h/17h is 40h 10 No Run Default value of EC Index 15h/16h/17h is 7Fh 01 Full Run Default value of EC Index 15h/16h/17h is 00h 00 75% Run Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1 Disable WDT to rest PWROK 0 Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1 Disable SVID Function 0 Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1 Enable Dual BIOS Function for GigaByte Only 0 Disable Dual BIOS Function for GigaByte Only



<18> VREF <<

<18> TMPIN1 <<

C113
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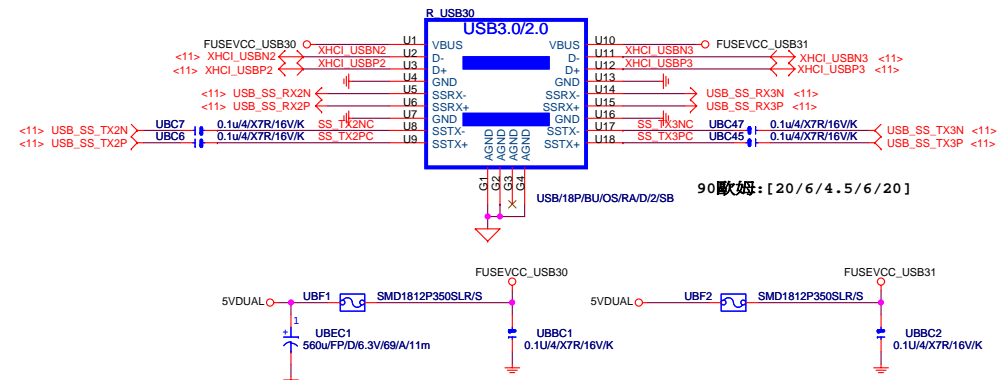
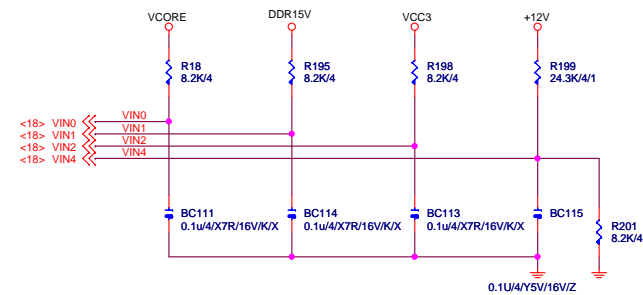
C114
0.1u4/X7R/16V/K

R203
10K/4/1

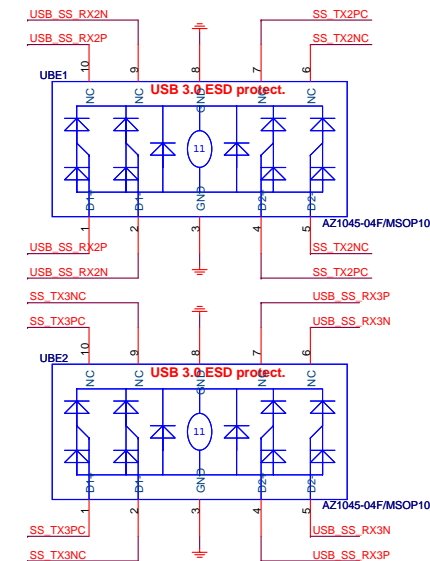
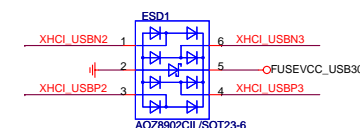
R206
8.2K/4/X

RS1
10K/1/4/S

SYSTEM
Thermistor



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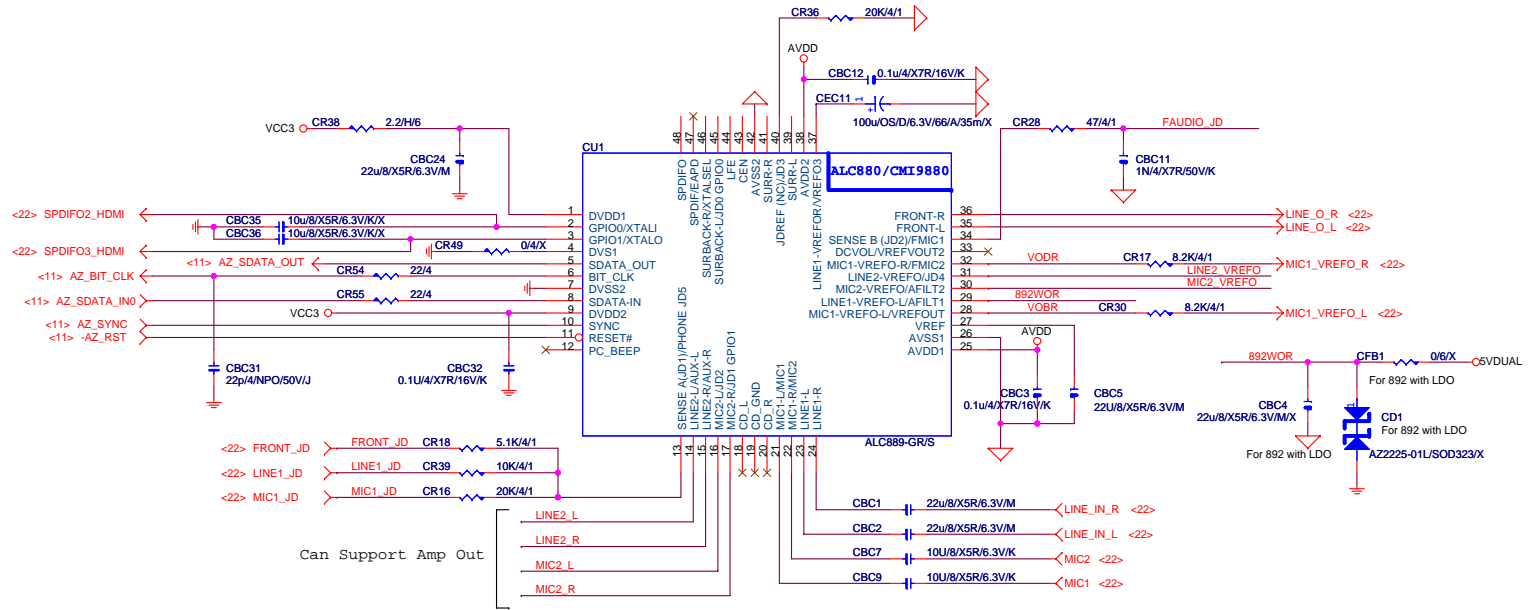
FAN , HWMO , R_USB30

Size	Document Number
Custom	GA-A75M-S2V

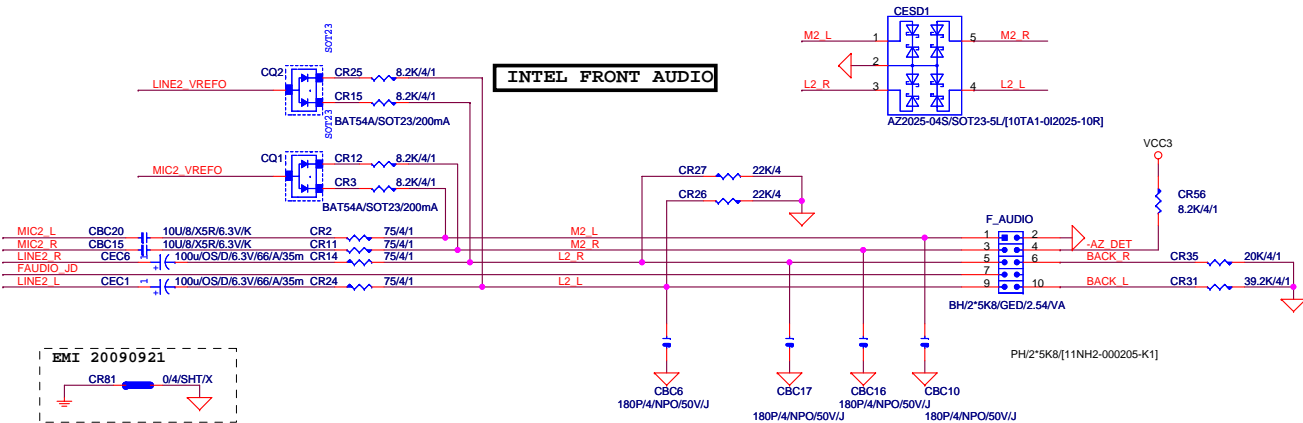
Rev	1.0
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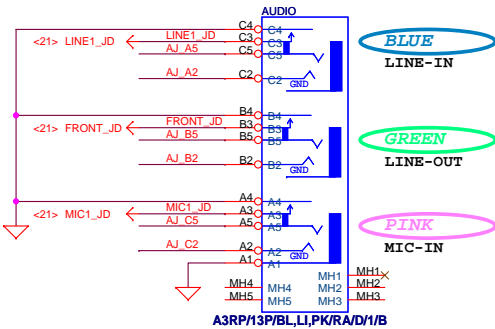
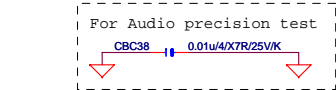
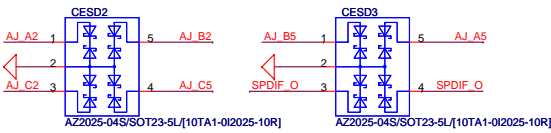
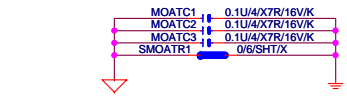
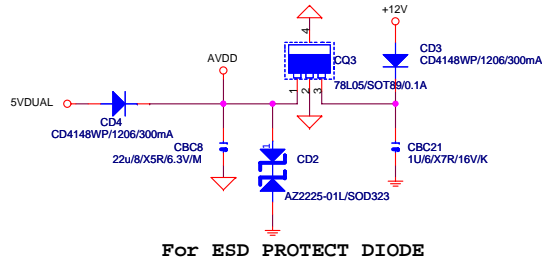
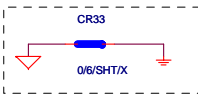
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	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



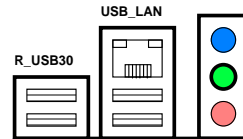
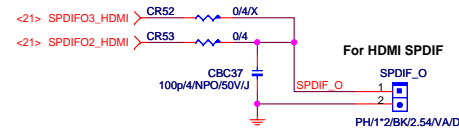
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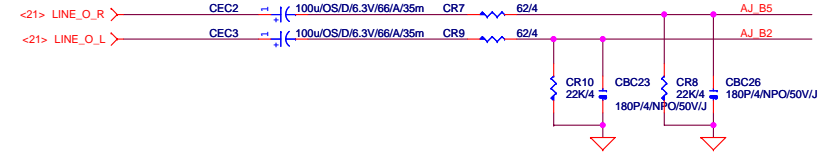


A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15P/[11NR6-403004-11]

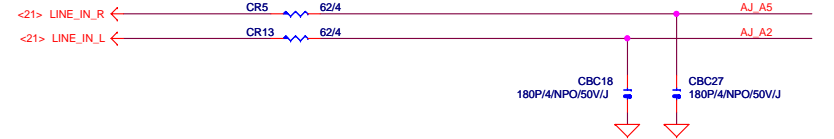
SPDIF



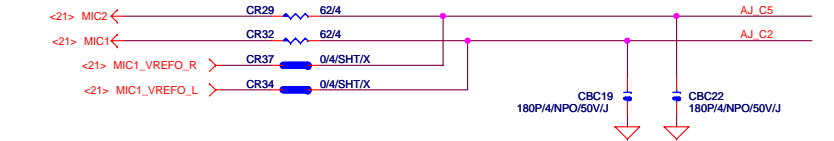
LINE OUT FRONT OUT



LINE-IN



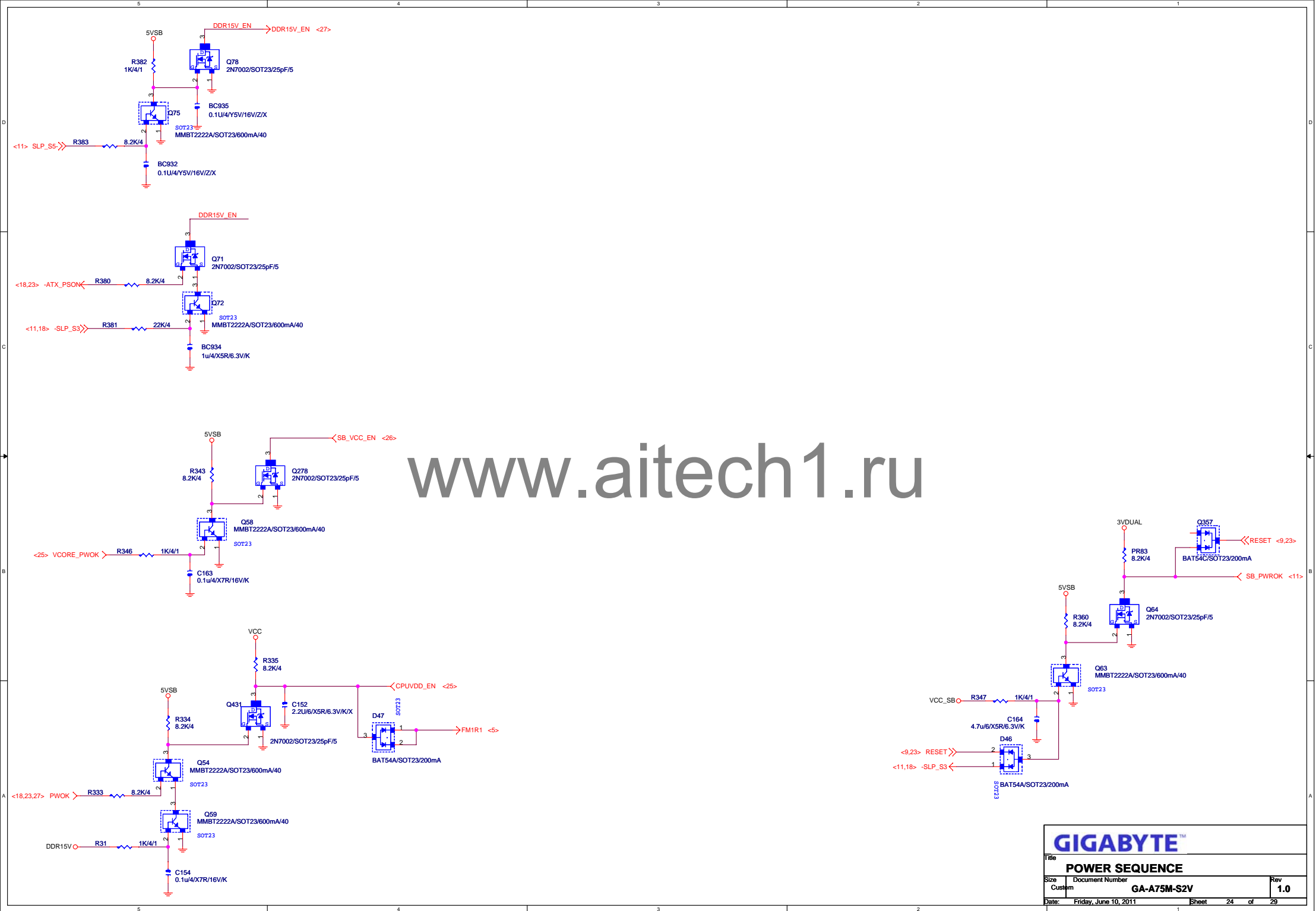
MIC

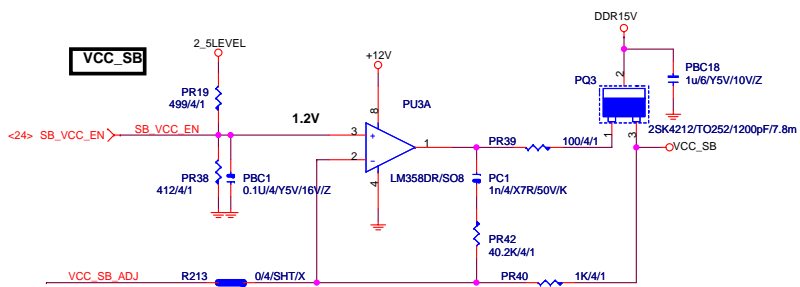


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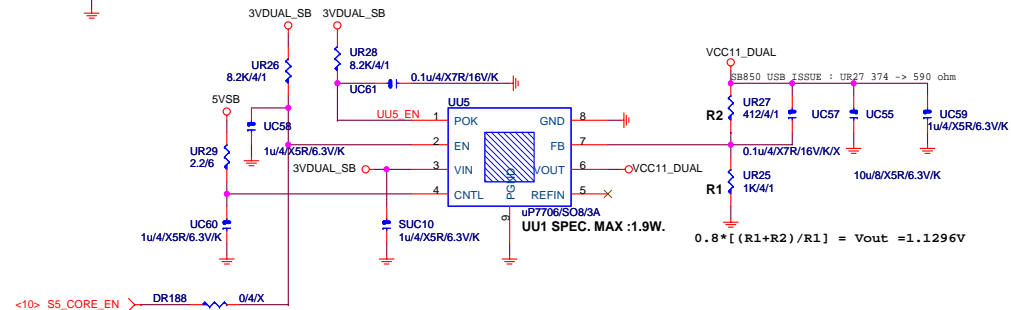
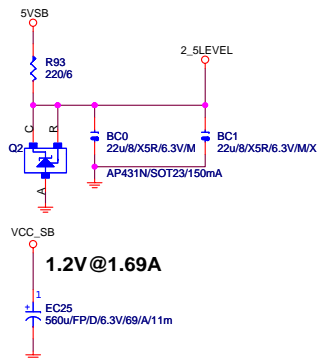
GIGABYTE™			
Title			
AUDIO JACK			
Size	Document Number	Rev	
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Date:	Friday, June 10, 2011	Sheet	22 of 29

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VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V



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